MAX+plus II Compiler Report File
Version 10.23 07/09/2003
Compiled: 03/18/2006 03:11:18

***** Project compilation was successful

** DEVICE SUMMARY **

Chip/ POF	Device	Input Pins	Output Pins	Bidir Pins	LCs	LCs % Utilized
jyankenunit						
	EPF8282ALC84-2	6	3	0	11	5 %
User Pins:		6	3	0		

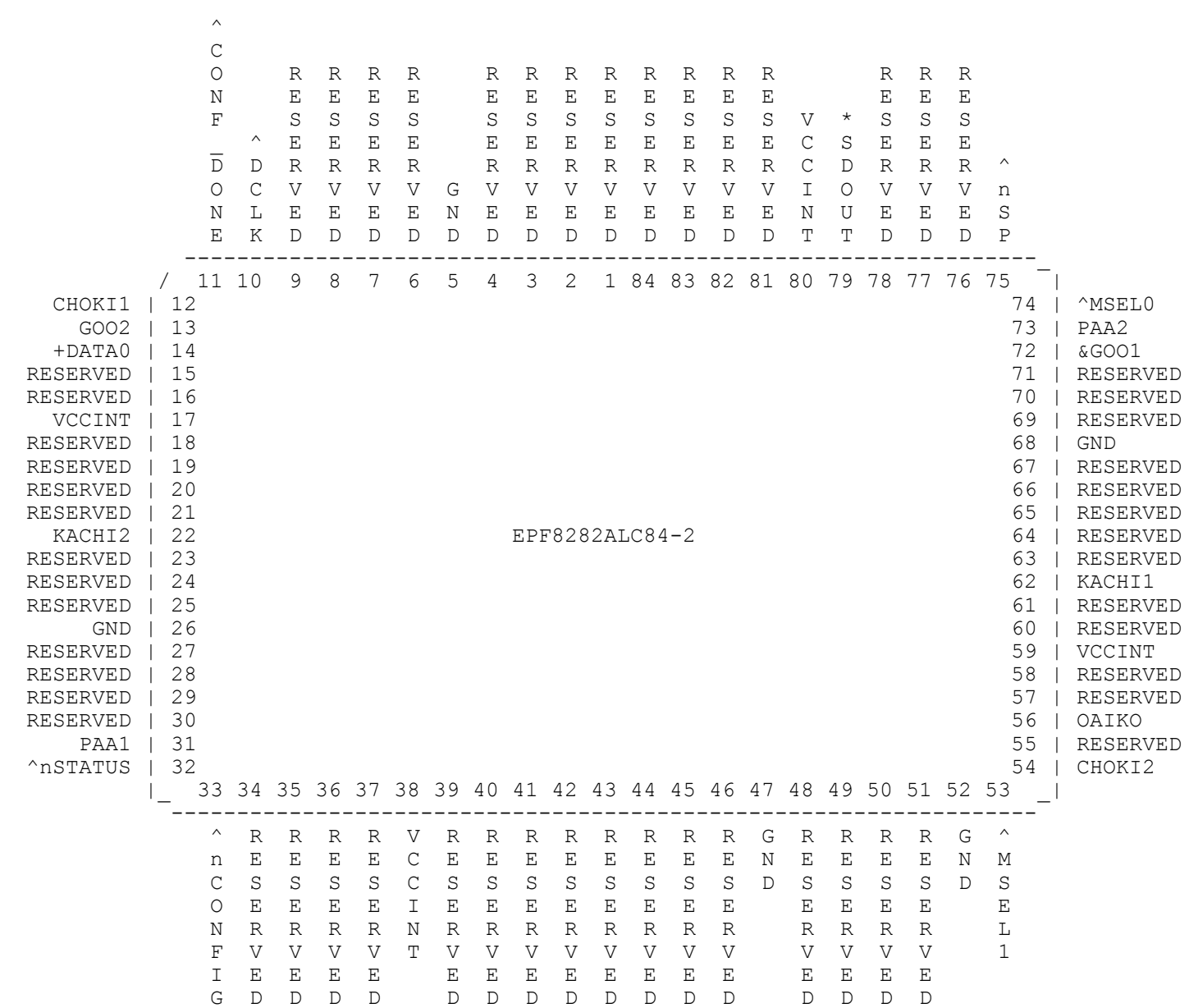
***** Logic for device 'jyankenunit' compiled without errors.

Device: EPF8282ALC84-2

FLEX 8000 Configuration Scheme: Active Serial

Device Options:

User-Supplied Start-Up Clock	= OFF
Auto-Restart Configuration on Frame Error	= OFF
Release Clears Before Tri-States	= OFF
Enable DCLK Output in User Mode	= OFF
Disable Start-Up Time-Out	= OFF
Enable JTAG Support	= OFF



N.C. = No Connect. This pin has no internal connection to the device.
VCCINT = Dedicated power pin, which MUST be connected to VCC (5.0 volts).
VCCIO = Dedicated power pin, which MUST be connected to VCC (5.0 volts).
GND = Dedicated ground pin or unused dedicated input, which MUST be connected to GND.
RESERVED = Unused I/O pin, which MUST be left unconnected.

^ = Dedicated configuration pin.
+ = Reserved configuration pin, which is tri-stated during user mode.
* = Reserved configuration pin, which drives out in user mode.
PDn = Power Down pin.
@ = Special-purpose pin.

= JTAG Boundary-Scan Testing/In-System Programming or Configuration Pin. The JTAG inputs TMS and TDI should be tied to VCC and TCK should be tied to GND when not in use.
& = JTAG pin used for I/O. When used as user I/O, JTAG pins must be kept stable before and during configuration. JTAG pin stability prevents accidental loading of JTAG instructions.

** RESOURCE USAGE **

Logic Array Block	Logic Cells	Column Interconnect Driven	Row Interconnect Driven	Clocks	Clears/ Presets	External Interconnect
B1	7/ 8(87%)	0/ 8(0%)	2/ 8(25%)	0/2	0/2	6/24(25%)
B2	4/ 8(50%)	0/ 8(0%)	1/ 8(12%)	0/2	0/2	6/24(25%)

Total dedicated input pins used:	4/4	(100%)
Total I/O pins used:	7/64	(10%)
Total logic cells used:	11/208	(5%)
Average fan-in:	3.72/4	(93%)
Total fan-in:	41/832	(4%)

Total input pins required:	6
Total input I/O cell registers required:	0
Total output pins required:	3
Total output I/O cell registers required:	0
Total buried I/O cell registers required:	0
Total bidirectional pins required:	0
Total reserved pins required	2
Total logic cells required:	11
Total flipflops required:	0
Total logic cells in carry chains:	0
Total number of carry chains:	0
Total logic cells in cascade chains:	0
Total number of cascade chains:	0

Synthesized logic cells:	5/ 208	(2%)	

Logic Cell Counts

Column:	01	02	03	04	05	06	07	08	09	10	11	12	13	Total
A:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B:	7	4	0	0	0	0	0	0	0	0	0	0	0	11
Total:	7	4	0	0	0	0	0	0	0	0	0	0	0	11

Device-Specific Information: f:\max2work\jyankenunit.rpt
jyankenunit

** INPUTS **

Pin	LC	Row	Col	Primitive	Code	Fan-In INP	Fan-In FBK	Fan-Out OUT	Fan-Out FBK	Name
12	-	-	--	INPUT		0	0	0	6	CHOKI1
54	-	-	--	INPUT		0	0	0	5	CHOKI2
72	-	A	--	INPUT		0	0	0	6	GOO1
13	-	A	--	INPUT		0	0	0	5	GOO2
31	-	-	--	INPUT		0	0	0	5	PAA1
73	-	-	--	INPUT		0	0	0	5	PAA2

Code:

s = Synthesized pin or logic cell
+ = Synchronous flipflop
/ = Slow slew-rate output
! = NOT gate push-back
r = Fitter-inserted logic cell

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** OUTPUTS **

Pin	Fed By LC	Row	Col	Primitive	Code	Fan-In INP	Fan-In FBK	Fan-Out OUT	Fan-Out FBK	Name
62	-	B	--	OUTPUT		0	1	0	0	KACHI1
22	-	B	--	OUTPUT		0	1	0	0	KACHI2
56	-	B	--	OUTPUT		0	1	0	0	OAIKO

Code:

s = Synthesized pin or logic cell
+ = Synchronous flipflop
/ = Slow slew-rate output
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** BURIED LOGIC **

IOC	LC	Row	Col	Primitive	Code	Fan-In INP	Fan-In FBK	Fan-Out OUT	Fan-Out FBK	Name
-	3	B	02	AND2	s	3	0	0	1	~9~1
-	4	B	02	AND2		3	1	0	1	:9
-	2	B	02	OR2	s	4	0	0	1	~11~1
-	1	B	02	OR2		2	2	1	0	:11
-	7	B	01	OR2	s	4	0	0	1	~31~1
-	2	B	01	OR2		2	2	1	0	:31
-	6	B	01	AND2		2	1	0	1	:32
-	5	B	01	OR2	s	4	0	0	1	~43~1
-	1	B	01	OR2		2	2	1	0	:43
-	4	B	01	AND2	s	4	0	0	2	~44~1
-	3	B	01	AND2		2	1	0	1	:44

Code:

s = Synthesized pin or logic cell
+ = Synchronous flipflop
/ = Slow slew-rate output
! = NOT gate push-back
r = Fitter-inserted logic cell

** FASTTRACK INTERCONNECT UTILIZATION **

Row FastTrack Interconnect:

Row	FastTrack Interconnect	Input Pins	Output Pins	Bidir Pins
A:	0/168(0%)	2/16(12%)	1/16(6%)	0/16(0%)
B:	5/168(2%)	0/16(0%)	3/16(18%)	0/16(0%)

Column FastTrack Interconnect:

Column	FastTrack Interconnect	Input Pins	Output Pins	Bidir Pins
01:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
02:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
03:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
04:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
05:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
06:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
07:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
08:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
09:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
10:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
11:	0/16(0%)	0/4(0%)	1/4(25%)	0/4(0%)
12:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)
13:	0/16(0%)	0/4(0%)	0/4(0%)	0/4(0%)

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** EQUATIONS **

CHOKI1   : INPUT;
CHOKI2   : INPUT;
GOO1     : INPUT;
GOO2     : INPUT;
PAA1     : INPUT;
PAA2     : INPUT;

-- Node name is 'KACHI1'
-- Equation name is 'KACHI1', type is output
KACHI1   =  _LC1_B2;

-- Node name is 'KACHI2'
-- Equation name is 'KACHI2', type is output
KACHI2   =  _LC2_B1;

-- Node name is 'OAIKO'
-- Equation name is 'OAIKO', type is output
OAIKO    =  _LC1_B1;

-- Node name is '~9~1'
-- Equation name is '~9~1', location is LC3_B2, type is buried.
-- synthesized logic cell
_LC3_B2  = LCELL( _EQ001);
  _EQ001 = !CHOKI2 & !PAA1 &  PAA2;

-- Node name is ':9'
-- Equation name is '_LC4_B2', type is buried
_LC4_B2  = LCELL( _EQ002);
  _EQ002 =  CHOKI1 & !GOO1 & !GOO2 &  _LC3_B2;

-- Node name is '~11~1'
-- Equation name is '~11~1', location is LC2_B2, type is buried.
-- synthesized logic cell
_LC2_B2  = LCELL( _EQ003);
  _EQ003 = !CHOKI2 & !GOO1 &  GOO2 &  PAA1
         #  CHOKI2 &  GOO1 & !GOO2 & !PAA1;

-- Node name is ':11'
-- Equation name is '_LC1_B2', type is buried
_LC1_B2  = LCELL( _EQ004);
  _EQ004 =  _LC4_B2
         # !CHOKI1 &  _LC2_B2 & !PAA2;

-- Node name is '~31~1'
-- Equation name is '~31~1', location is LC7_B1, type is buried.
-- synthesized logic cell
_LC7_B1  = LCELL( _EQ005);
  _EQ005 = !CHOKI2 &  GOO1 & !PAA1 &  PAA2
         #  CHOKI2 & !GOO1 &  PAA1 & !PAA2;

-- Node name is ':31'
-- Equation name is '_LC2_B1', type is buried
_LC2_B1  = LCELL( _EQ006);
  _EQ006 = !CHOKI1 & !GOO2 &  _LC7_B1
         #  _LC6_B1;

-- Node name is ':32'
-- Equation name is '_LC6_B1', type is buried
_LC6_B1  = LCELL( _EQ007);
  _EQ007 =  CHOKI1 & !GOO1 &  _LC4_B1;

-- Node name is '~43~1'
-- Equation name is '~43~1', location is LC5_B1, type is buried.
-- synthesized logic cell
_LC5_B1  = LCELL( _EQ008);
  _EQ008 = !CHOKI1 & !CHOKI2 &  PAA1 &  PAA2
         #  CHOKI1 &  CHOKI2 & !PAA1 & !PAA2;

-- Node name is ':43'
-- Equation name is '_LC1_B1', type is buried
_LC1_B1  = LCELL( _EQ009);
  _EQ009 = !GOO1 & !GOO2 &  _LC5_B1
         #  _LC3_B1;
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-- Node name is '~44~1'
-- Equation name is '~44~1', location is LC4_B1, type is buried.
-- synthesized logic cell
_LC4_B1  = LCELL( _EQ010);
  _EQ010 = !CHOKI2 &  GOO2 & !PAA1 & !PAA2;

-- Node name is ':44'
-- Equation name is '_LC3_B1', type is buried
_LC3_B1  = LCELL( _EQ011);
  _EQ011 = !CHOKI1 &  GOO1 &  _LC4_B1;
```

Project Information f:\max2work\jyankenunit.rpt

** COMPILATION SETTINGS & TIMES **

Processing Menu Commands

Design Doctor = off

Logic Synthesis:

Synthesis Type Used = Multi-Level

Default Synthesis Style = NORMAL

Logic option settings in 'NORMAL' style for 'FLEX8000' family

CARRY_CHAIN = ignore
CARRY_CHAIN_LENGTH = 32
CASCADE_CHAIN = ignore
CASCADE_CHAIN_LENGTH = 2
DECOMPOSE_GATES = on
DUPLICATE_LOGIC_EXTRACTION = on
MINIMIZATION = full
MULTI_LEVEL_FACTORING = on
NOT_GATE_PUSH_BACK = on
REDUCE_LOGIC = on
REFACTORIZATION = on
REGISTER_OPTIMIZATION = on
RESYNTHESIZE_NETWORK = on
SLOW_SLEW_RATE = off
SUBFACTOR_EXTRACTION = on
IGNORE_SOFT_BUFFERS = on
USE_LPM_FOR_AHDL_OPERATORS = off

Other logic synthesis settings:

Automatic Global Clock = on
Automatic Global Clear = on
Automatic Global Preset = on
Automatic Global Output Enable = on
Automatic Fast I/O = off
Automatic Register Packing = off
Automatic Open-Drain Pins = on
Automatic Implement in EAB = off
Optimize = 5

Default Timing Specifications: None

Cut All Bidir Feedback Timing Paths = on
Cut All Clear & Preset Timing Paths = on

Ignore Timing Assignments = on

Functional SNF Extractor = off

Linked SNF Extractor = off
Timing SNF Extractor = on
Optimize Timing SNF = off
Generate AHDL TDO File = off
Fitter Settings = NORMAL
Smart Recompile = off
Total Recompile = off

Interfaces Menu Commands

EDIF Netlist Writer = off
Verilog Netlist Writer = off
VHDL Netlist Writer = off

Compilation Times

Compiler Netlist Extractor 00:00:01
Database Builder 00:00:00
Logic Synthesizer 00:00:00
Partitioner 00:00:00

Fitter	00:00:00
Timing SNF Extractor	00:00:00
Assembler	00:00:00
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Total Time	00:00:01

Memory Allocated

Peak memory allocated during compilation = 6,130K